

# MICRON

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Date: 6/28/99  
Time: 7:15 pm eastern  
Pages: 6 (including cover sheet)

**TO:** Examiner Kim, Art unit 2751

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**FROM:**

Name: Charles Brantley  
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**MESSAGE:** The documents you requested concerning the February '99  
IDS follow.

Charles Brantley

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**In re application of:  
Mailloux, et al.**

Serial No.: 08650,719

Filed: May 20, 1996

**For: BURST/PIPELINED EDO  
MEMORY DEVICE**

§§ Group Art Unit: 2751

§ Examiner: Kim, H.

§ Atty. Docket: 95-0653.0

Fax Received

JUN 28 1999

## Group 2700

## **INFORMATION DISCLOSURE STATEMENT**

**Assistant Commissioner for Patents  
Washington, D.C. 20231**

Dear Sir:

In compliance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant[s] respectfully request[s] that this Information Disclosure Statement be entered and that the references listed on the attached Form PTO-1449 be considered by the Examiner and made of record.

In accordance with 37 C.F.R. § 1.97(b), this Information Disclosure Statement is not to be construed as a representation that a search has been made or that no other possible material information as defined in 37 C.F.R. § 1.56(a) exists.

The following references are submitted for the Examiner's review:

## U.S. Patents

<u>U.S. Patent No.</u>	<u>Issue Date</u>	<u>Inventor</u>
5,652,724	7/97	Manning
5,457,659	10/95	Schaefer
5,452,261	9/95	Chung et al.

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5,682,354	10/97	Manning
5,640,364	06/97	Merritt et al.
5,729,504	12/95	Cowles
5,661,695	08/97	Zagar et al.
5,305,284	04/94	Iwase
5,325,330	06/94	Morgan
5,325,502	06/94	McLaury
5,373,227	12/94	Keeth
5,410,670	04/95	Hansen et al.
5,349,566	09/94	Merritt et al.
5,668,773	09/97	Zagar et al.
4,870,622	09/89	Aria et al.
5,058,066	10/91	Yu
5,280,594	01/94	Young et al.

Other References

Micron Technology, Inc. , "1995 DRAM Data Book" pp. 4-1 thru 4-42, 12/95.

"Rossini, Pentium, PCI-ISA, Chip Set", Symphony Laboratories, entire book.

Related Co-pending Applications

PCT Patent Application No. PCT/US95/16656, filed 12/21/1995, entitled: Burst Edo Memory Device

Address Counter.

PCT Patent Application No. PCT/US95/16984 , filed 12/22/1995, entitled: Burst Edo Memory Device.

This Information disclosure Statement is being submitted after the mailing of the first Office Action, but before the mailing of a Final Rejection or Notice of Allowance. The Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) of \$240.00 and any additional fees which may be required to Micron Technology, Inc. Deposit Account No. 13-3092, Order No. 95-0653.00.

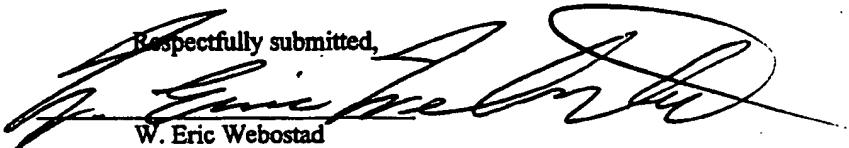
If there are any matters which may be resolved or clarified through telephone interview, the Examiner is respectfully requested to contact Applicant's undersigned attorney at the number indicated.

\* \* \*

A Form PTO-1449 is enclosed herewith.

Date: 2-18-99

Respectfully submitted,

  
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1. 5,652,724, Jul. 29, 1997, Burst EDO memory device having pipelined output buffer; Troy A. Manning, 365/189.05, 233 [IMAGE AVAILABLE]
2. 5,457,659, Oct. 10, 1995, Programmable dynamic random access memory (DRAM); Scott Schaefer, 365/222, 189.05, 191, 193, 230.03, 238.5 [IMAGE AVAILABLE]
3. 5,452,261, Sep. 19, 1995, Serial address generator for burst memory; Jinyong Chung, et al., 365/233, 221, 230.06, 230.08, 236, 239 [IMAGE AVAILABLE]
4. 5,280,594, Jan. 18, 1994, Architecture for high speed contiguous sequential access memories; Elvan S. Young, et al., 711/157; 364/239, 239.51, 244, 247, DIG.1; 365/230.04 [IMAGE AVAILABLE]
5. 5,058,066, Oct. 15, 1991, Output buffer precharge circuit for DRAM; Jaiwhan Yu, 365/189.05, 203 [IMAGE AVAILABLE]
6. 4,870,622, Sep. 26, 1989, DRAM controller cache; Percy R. Aria, et al., 365/230.02, 230.03, 238.5 [IMAGE AVAILABLE]
7. 5,668,773, Sep. 16, 1997, Synchronous burst extended data out DRAM; Paul S. Zagar, et al., 365/233, 233.5 [IMAGE AVAILABLE]
8. 5,325,502, Jun. 28, 1994, Pipelined SAM register serial output; Loren L. McLaury, 711/169; 364/244.8, 249.2, 251.4, 261.8, DIG.1 [IMAGE AVAILABLE]
9. 5,373,227, Dec. 13, 1994, Control circuit responsive to its supply voltage level; Brent Keeth, 323/313, 274, 299; 327/72, 74, 541 [IMAGE AVAILABLE]
10. 5,410,670, Apr. 25, 1995, Accessing system that reduces access times due to transmission delays and I/O access circuitry in a burst mode random access memory; Craig C. Hansen, et al., 711/169; 364/961.3, 964.26, 964.33, DIG.2; 365/189.01, 230.01 [IMAGE AVAILABLE]
11. 5,349,566, Sep. 20, 1994, Memory device with pulse circuit for timing data output, and method for outputting data; Todd A. Merritt, et al., 365/233.5, 189.05, 191, 193 [IMAGE AVAILABLE]
12. 5,682,354, Oct. 28, 1997, CAS recognition in burst extended data out DRAM; Troy Manning, 365/233.5, 235, 236, 238.5, 239 [IMAGE AVAILABLE]
13. 5,640,364, Jun. 17, 1997, Self-enabling pulse trapping circuit; Todd Merritt, et al., 365/233.5, 206, 230.08 [IMAGE AVAILABLE]
14. 5,729,504, Mar. 17, 1998, Continuous burst edo memory device; Timothy B. Cowles, 365/236, 238.5, 239; 711/169 [IMAGE AVAILABLE]
15. 5,661,695, Aug. 26, 1997, Burst EDO memory device; Paul S. Zagar, et al., 365/233.5, 189.01, 238.5 [IMAGE AVAILABLE]
16. 5,305,284, Apr. 19, 1994, Semiconductor memory device; Taira Iwase, 365/238.5, 189.05, 233.5 [IMAGE AVAILABLE]
17. 5,325,330, Jun. 28, 1994, Memory circuit with foreshortened data output signal; Donald M. Morgan, 365/189.05, 189.01, 203, 230.01 [IMAGE AVAILABLE]